TUGRUL EFESOY 571-469-7597 | tbakiefesoy03@gmail.com | linkedin.com/in/tugrul-efesoy/ | Website

SUMMARY OF QUALIFICATIONS

• Proven expertise in digital hardware design spanning FPGA/RTL, pipelined CPU architectures in SystemVerilog, and transistor-level CMOS with full VLSI layout and timing constraint closure
• Hands-on analog and embedded systems background including op-amp signal conditioning, RC/RL filter design, PCB layout in KiCad, and LTspice simulation with oscilloscope-based hardware validation
• Embedded firmware in C with FreeRTOS and I2C/SPI on ESP32; experienced in CAN/J1939 with CANalyzer debugging and MATLAB/Simulink HIL testing, reducing validation cycle time by 30%
• Founder of two nationwide organizations with proven impact across 1000+ students; built and scaled an AI-powered full-stack platform reaching 300M+ views in one year

EDUCATION

University of Washington Seattle, WA *Expected June 2026*
B.Sc. Electrical and Computer Engineering
GPA: 3.6, Dean's List (six quarters)
Related Coursework: Embedded Systems, Computer Architecture, Digital Circuits & Systems EV Charging Systems, CAN & Vehicle Networks, VLSI Design, CMOS & Transistor-Level Design, Signal Processing, Circuits & Electronics, Op-Amps, Filters & Transforms

RELEVANT EXPERIENCE

Project Lead, High Voltage EV Charging Integration, *Paccar Mount Vernon, WA* *Dec 2025 - Present*
• Led the integration of a 650V EV charging system with J1939 CAN communication, connecting HV/LV battery systems and dual Charge Control Units to enable safe, coordinated power flow
• Programmed C-based control logic and diagnostics over CAN, using CANalyzer to trace signal paths, resolve ECU sync issues, and validate safety logic in real-time conditions
• Developed and executed a full Hardware-in-the-Loop validation pipeline using MATLAB/Simulink and real hardware, reducing testing time by 30% while improving fault detection

Intern, FPGA & Digital Design, *PnCEL Lab* *June 2025 – Aug 2025*
• Designed and verified pipelined CPU architectures in SystemVerilog, implementing forwarding and hazard control to optimize timing and instruction throughput in FPGA/SoC designs
• Completed full VLSI layout of a 16-bit CMOS design across 5 metal layers with timing constraint closure, integrated into a broader SoC design flow
• Validated RTL designs through FPGA synthesis and simulation; analyzed waveforms and timing reports to identify and resolve critical path violations

Undergraduate Research Assistant – Analog & Embedded Systems, *University of Washington* *Sep 2024 – Mar 2025*
• Designed a real-time multi-sensor data acquisition system on ESP32 using FreeRTOS, implementing priority-based task scheduling for concurrent SPI and I2C sensor communication with interrupt-driven reads
• Integrated analog front-end signal conditioning including op-amp buffering and RC low-pass filtering before ADC sampling, bridging analog circuit design with embedded firmware in a single end-to-end pipeline
• Validated signal integrity and real-time task performance using oscilloscope and logic analyzer

PROJECTS & ENTREPRENEURSHIP

Founder & Engineer, TBE Academy *Jan 2025 – Present*
• Built a full-stack web platform from scratch serving 1000+ students nationally; integrated AI-driven content pipelines, automated outreach systems, and real-time data tracking
• Grew platform to 300M+ views in one year through AI-powered content generation and automation; mentored 4 students into top university placements; featured in national media

AI Training & Automation Projects *Mar 2025 – Present*
• Fine-tuned AI models for content generation and built automated pipelines to scale platform operations

President, Turkish Student Association, *University of Washington* *Oct 2022 – Present*